

AMENDMENT UNDER 37 C.F.R. § 1.111  
U.S. Application No. 10/519,457

Attorney Docket No. Q85448

**AMENDMENTS TO THE DRAWINGS**

Applicant is submitting new Figures 1 and 2 that include a legend designated of Prior Art. Therefore, Applicant respectfully submits that the corrected drawing sheets are in compliance with 37 C.F.R. 1.121(d). Thus, the Examiner is requested to approve the new drawings.

Attachment: Replacement Sheets

**REMARKS**

Claims 1-14 are all the claims pending in the application.

Claims 2-12 are withdrawn.

Applicant thanks the Examiner acknowledging drawings filed on December 29, 2004, and acknowledging the claim for priority under 35 U.S.C. § 119, and receipt of all certified copies of the priority documents submitted.

Also, the Applicant thanks the Examiner for considering the references cited in IDS filed on December 29, 2004.

**Drawings**

The Examiner objects to the drawings because figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. MPEP § 608.02(g) Applicant is submitting corrected drawings that are labeled as "Prior Art." Therefore, the Examiner is requested to approve the drawings and withdraw the drawing objections.

**Claim Objections**

Claims 1, 13 , and 14 have been corrected as requested by the Examiner. Thus withdrawal of this objection is respectfully requested.

**Claim Rejection - 35 U.S.C. § 102**

Claim 1 has been rejected under 35 U.S.C. § 102(b) as being anticipated by Taiichi (JP 07-273610). Applicant traverse this rejection because Taiichi fails to disclose or suggest all of the claim limitations. Specifically, Taiichi fails to disclose or suggest the following:

**Claim 1:**

a master circuit comprising a first data reading differential pair, a first data-hold differential pair comprising transistors of a size smaller than transistors comprising the first data reading differential pair, and a first current source circuit connected to the first data reading differential pair and the first data-hold differential pair; and

a slave circuit comprising a second data reading differential pair, a second data-hold differential pair comprising of transistors of a size smaller than transistors

comprising the second data reading differential pair, and a second current source circuit connected to the second data reading differential pair and the second data-hold differential pair;

The Examiner alleges that Taiichi discloses a first current source circuit (X7) connected to the first data reading differential pair and the first data-hold differential pair. (Office Action page 3) However, Taiichi actually discloses separating the current path of the differential logical circuit for the data read-out, and the differential logical circuit for data-hold. This is done on both, the master side and the slave side. (par 0015). These separate current sources are shown in figure 1 of Taiichi, where the current source for transistor X7 is tied only to the data read-out circuit for both the master and the slave side, and where the current source for transistor XL7 is tied only to the differential logic circuit for the data-hold for both the master and the slave side. Therefore, Taiichi fails disclose the claimed invention of a first current source circuit connected to the first data reading differential pair and the first data-hold differential pair.

Applicants also note that Taiichi has the same problems as the art cited in the Background section. Specifically, it has a circuit configuration, that, not only complicates the circuit layout, but also increases the number of crossovers between signal lines, hence increasing parasitic capacitance between signal lines (Fig. 2; and page 6, lines 2-4).

Furthermore, the Examiner fails to address the claim limitation of a second current source circuit connected to the second data reading differential pair and the second data-hold differential pair.

Therefore, at least for these reason, Applicant respectfully submits that independent claim 1 is patentable over the applied reference.

Further, Applicant respectfully submits that rejected claim 13 and 14 are allowable, at least because of their dependency.

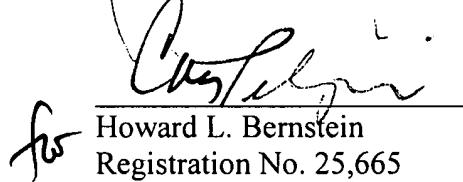
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In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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